# PCB Layout and Design Considerations for the CH7301C DVI Output Device

## 1. Introduction

This application note focuses on basic PCB layout and design guidelines for the CH7301C DVI Output Device. Guidelines in component placement, power supply decoupling, grounding, input signal interface and video components for DVI link implementation, are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 64-pin LQFP package of CH7301C. Please refer to CH7301C data sheet for the details of the pin assignments.

## 2. Component Placement and Design Considerations

Components associated with the CH7301C DVI transmitter should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

### 2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C7, C8, C9, C11, C12, C14, C17) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7301C ground pins, in addition to ground vias.

#### 2.1.1 Ground Pins

The analog and digital grounds of the CH7301C should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7301C ground pins should connect directly to its respective decoupling capacitor ground lead, then connect the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the ground pins assignment.

#### 2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage DVDDV), DVI, Analog, and DAC power planes are recommended. See **Table 1** for the Power supply pins assignment.

**Table 1: Power Supply Pins Assignment in CH7301C**

| Pin # | # of Pins | Type | Symbol | Description |
|---|---|---|---|---|
| 1, 12, 49 | 3 | Power | DVDD | **Digital Supply Voltage (3.3V)** |
| 6, 11, 64 | 3 | Power | DGND | **Digital Ground** |
| 45 | 1 | Power | DVDDV | **I/O Supply Voltage (1.1V to 3.3V)** |
| 23, 29 | 2 | Power | TVDD | **DVI Transmitter Supply Voltage (3.3V)** |
| 20, 26, 32 | 3 | Power | TGND | **DVI Transmitter Ground** |
| 18 | 1 | Power | AVDD | **PLL Supply Voltage (3.3V)** |
| 17 | 1 | Power | AGND | **PLL Ground** |
| 33 | 1 | Power | VDD | **DAC Supply Voltage (3.3V)** |
| 34, 40 | 2 | Power | GND | **DAC Ground** |

- **DVDDV & VREF Decoupling and Connection**

VREF is used as a reference level for pixel data input D[11:0], HSYNC input and VSYNC input. Please refer to **Figure 1** for optimum decoupling. In general applications, VREF is derived from DVDDV divided by 2, i.e., VREF = 1/2 x DVDDV.

Therefore, in **Figure 2**, both resistors should have the same value (10KΩ@ 1%). The decoupling capacitor is required as shown in **Figure 2**. Also, the DVDDV voltage supply should be connected to the graphics controller I/O supply voltage.

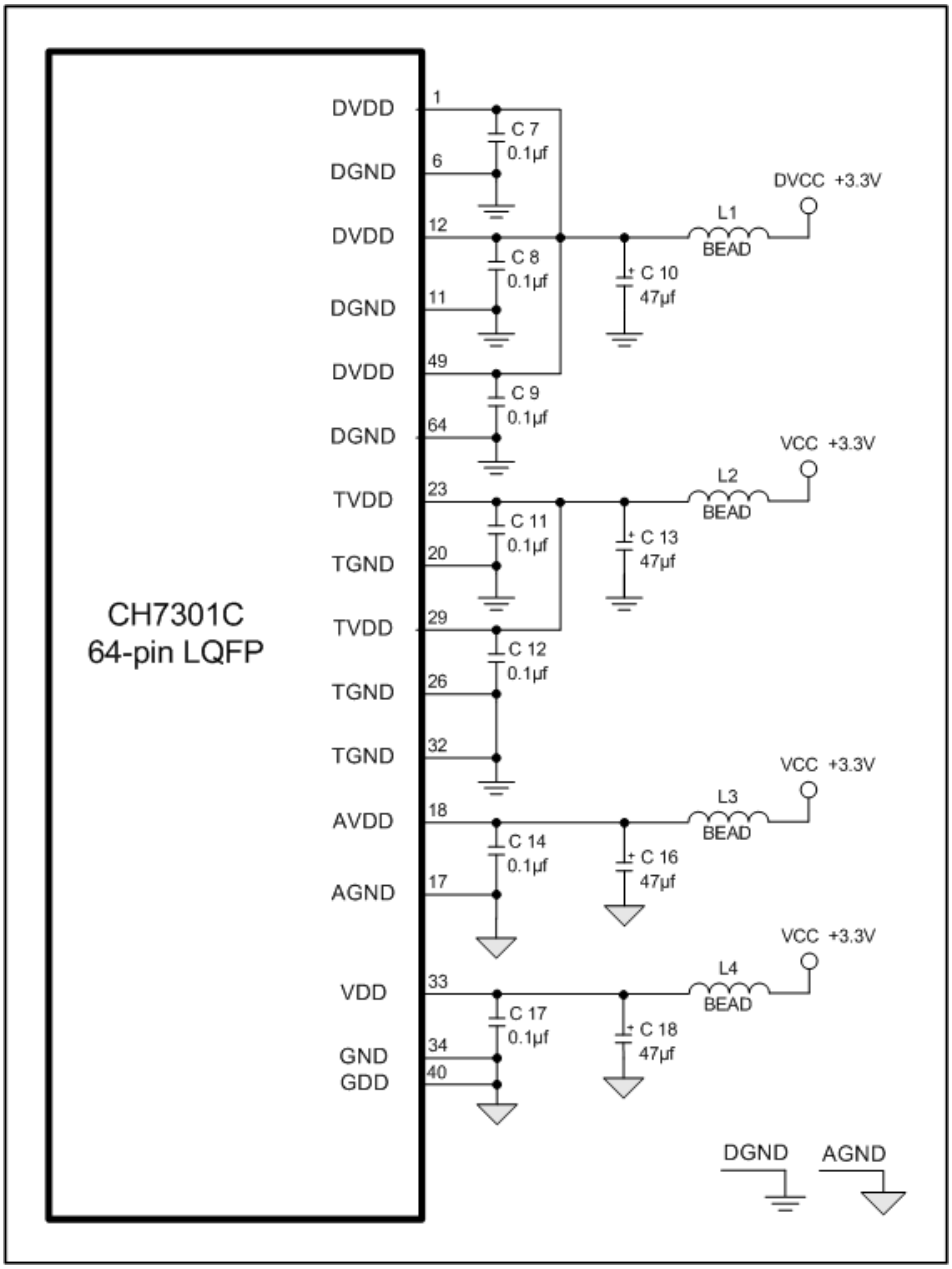



**Figure 1: Power Supply Decoupling and Distribution**

**Notes:** All the Ferrite Beads described in this document are recommended to have an impedance of less then 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please use Fair_Rite part# 2743019447 or an equivalent ferrite bead.

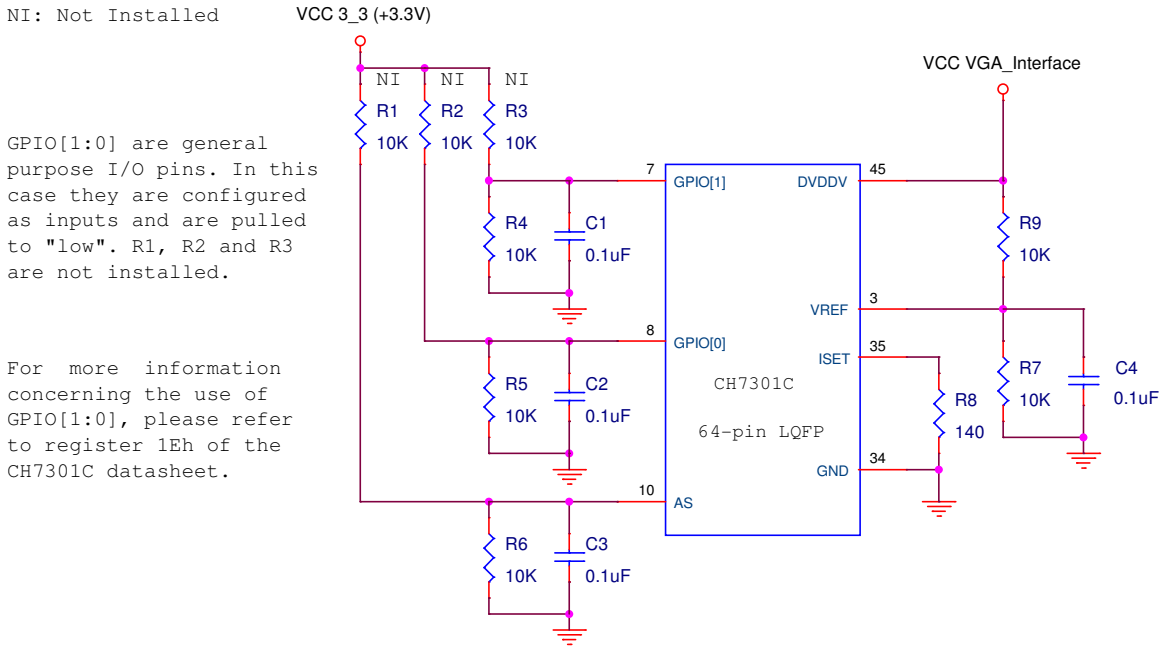



**Figure 2: ISET, VREF, DVDDV, GPIO and AS connection**

## 2.2 General Control

- ### ISET pin

  The ISET pin, pin 35, sets the DAC current. A 140Ω resistor should be placed as close as possible to the ISET pin using short and wide traces. Whenever possible, the ISET resistor ground pin should also be connected to pin 34. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7301C. See **Figure 2** for design reference.

- ### Data Enable pin

  The Data Enable pin, pin 2, is an input pin and accepts the Data Enable signal from the VGA graphics chipset. Active video data is indicated when the VGA drives the Data Enable signal ‘high’. When the Data Enable signal is ‘low’, the video data will not be encoded and driven out of the DVI interface. The voltage levels are between 0V and DVDDV, and the VREF signal is used as the threshold level.

- ### GPIO [0] & GPIO[1] pins

  GPIO[1:0] are General Purpose I/O pins. To set the direction of these pins, register 1Eh, the GPIO Control Register must be set accordingly. The GPIO[1] pin can be configured as an output for the DVI link detect signal. In this configuration, this pin will be driven low when a termination change has been detected on the HPDET input.

- ### AS pin

  The Address Select pin, pin 10, can be configured as shown in **Figure 2**. This pin determines the serial port address of the device. If AS is pulled ‘low’, then the serial port address is 0x76h, if AS is pulled ‘high’, then the serial port address is 0x75h.

  Note: To use the Intel driver for the CH7301C, the AS pin must be pulled ‘low’.

- **Video Inputs (D[11:0])**

  Since the digital pixel data and the pixel clock of the CH7301C may toggle at speeds up to165MHz (depending on the input mode), it is critical that the connection of these video signals between the graphics controller and the CH7301C be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that 8 mil traces be used in routing these signals.

## 2.3 Serial Port Interface

- **SPD and SPC pins**

  SPD (pin 14) and SPC (pin 15) function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 2.2 KΩ resistors.

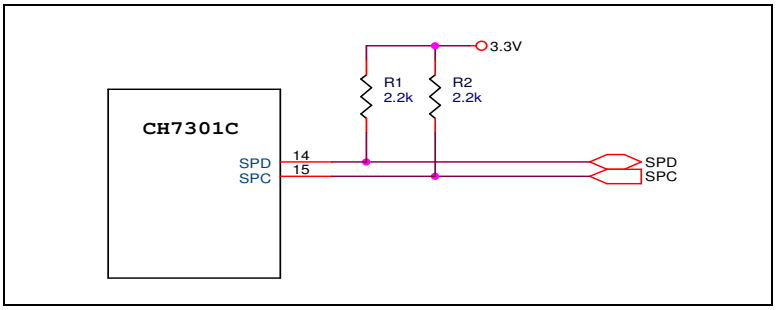



**Figure 3: Serial Port Interface**

## 2.4 DVI Output and Control

In DVI output mode, the multiplexed input data, sync and clock signals are input to the CH7301C from the graphics controller's digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

The TDC0, TDC1, TDC2 & TLC signals are high frequency differential signals that need to be routed with special precautions. Since the TDC0, TDC1, TDC2 & TLC signals are differential they must be routed in pairs: TDC0 & TDC0*, TDC1 & TDC1*, TDC2 & TDC2*, TLC & TLC* signals. The lengths of the 4 pair of signals must be kept as close to the same as possible. The maximum length difference must not exceed 100 mils for any of the pairs relative to each other. The number of bends should be kept to 4 or less and 45 degree is the maximum corner angle. These signals should be routed on the top layer directly to the DVI connector without any vias to the bottom layer. The pin placement of the TDC0, TDC1, TDC2 & TLC signals allows for a direct route to the DVI connector. The CH7301C is able to drive a DVI display at a pixel rate of up to 165 MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

**In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each DVI Output (data and clock).**

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel's recommended diode protection circuitry, using Semtech RClamp 0514M or

Semtech RClamp 0524P diode array devices, will protect the CH7301C DVI output from DVI panel discharges of greater than 8kV (contact) and 15kV (air). Both Semtech RClamp devices have low I/O to I/O capacitance. (RClamp 0514M = 0.7pF typical and RClamp 0524 = 0.3pF typical). This low capacitance will allow the DVI eye diagram to remain within specification.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has also confirmed that BAT54SLT1 diode device can protect pin 9 (HPDET) of the CH7301C from DVI panel discharges greater than 4kV (contact) and 8kV (air). It is also highly recommended to protect the DDCCLK and DDCDATA signals on the DVI connector.

**Figure 4** shows an example of the connection of the DVI output. In the figure a DVI-I Right Angle Connector is used to interface the CH7301C DVI outputs to the monitor.

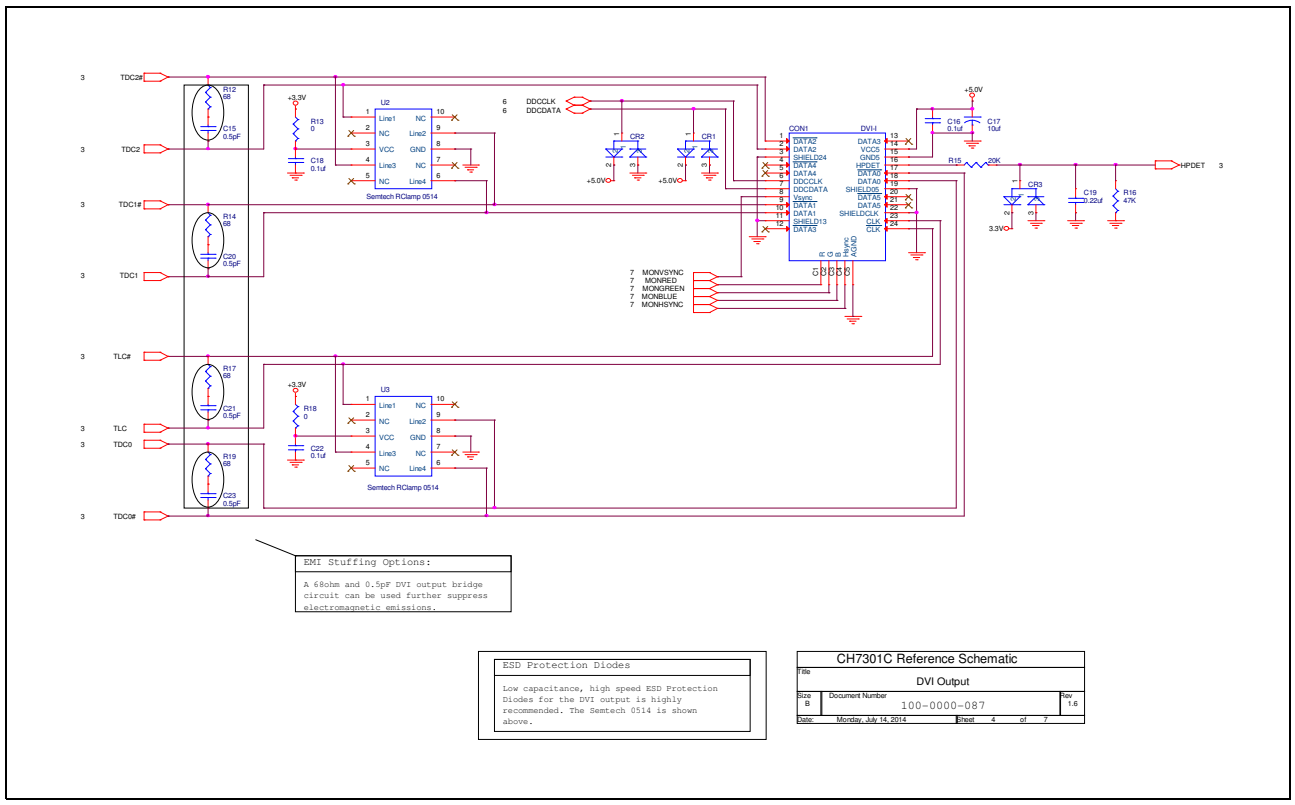



**Figure 4: DVI-I Output Connection**

- **DVI Link Detect Output (HPINT) (internal pull-up)**

The GPIO[1]/HPINT pin can be used to output the DVI link detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. To configure the GPIO[1]/HPINT pin to function as a HPINT, the GOENB1 ( reg 1Eh[7] ) and HPIE2 ( reg 20h[7] ) bits of the CH7301C must be set to 1. The HPINT function will pull low with an open drain output following a transition on the HPDET input.

- **DVI Data Channel (TDC[2:0] and TDC[2:0]*)**

These pins (Pins 28, 25, 22 for TDC[2:0] and Pins 27, 24, 21 for TDC[2:0]*) provide the DVI differential outputs for data channel 0 (blue), channel 1(green) and channel 2 (red) (See **Figure 4**).

- **DVI Link Clock Outputs (TLC and TLC*)**

  These pins (Pins 30, 31) provide the DVI differential clock outputs for the DVI interface corresponding to data on the TDC[2:0] outputs (See **Figure 4**).

- **HPDET (DVI Hot Plug Detect)**

  This input pin (Pin 9) determines whether the DVI link is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the GPIO[1]/HPINT pin pulling low (See **Figure 4**).

- **VSWING (DVI Link Swing Control)**

  This pin (Pin 19) sets the swing level of the DVI outputs. A 2.4KΩ resistor should be connected between this pin and GND using short and wide traces.

## 2.5 Analog RGB Output

The R, G, B (pins 38, 37, 39) signals are analog video signals. These signals should not be routed together. There should be a minimum of 12 mils spacing between each of the R, G, B signals and 20 mils spacing between them and any digital trace.

Typically these signals should be routed in a separate analog area without any digital signal running through the area. Corners for these traces should be at a maximum of 45 degree. 90 degree corners should not be used due to cross coupling between adjacent traces. These traces should be kept on the top layer to minimize the use of vias on them.

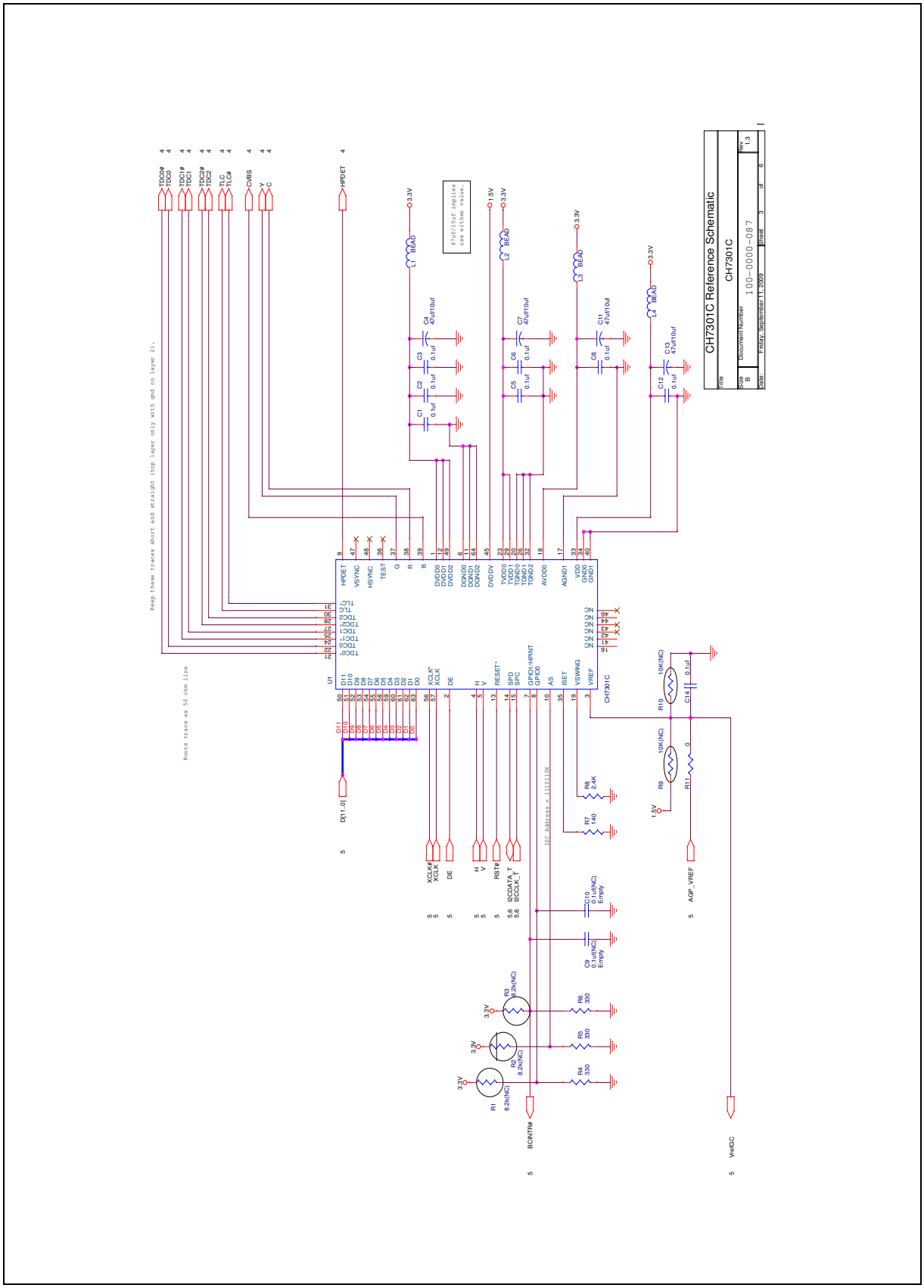
**In order to minimize the hazard of ESD, it is highly recommended to use ESD protection diodes for each of the Analog RGB signals.**

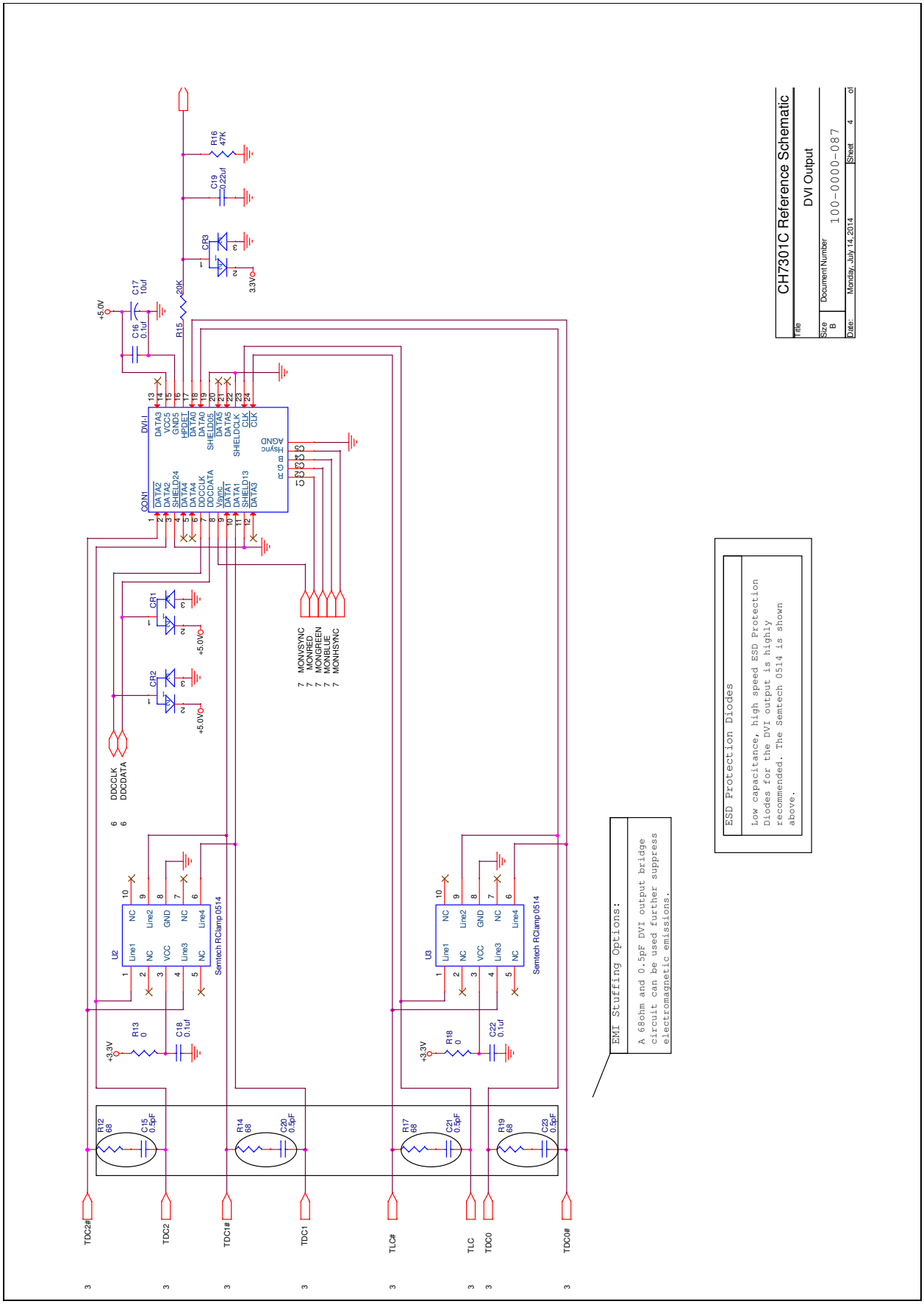
In **Figure 4**, the input protection diodes D1 - D6 should be placed as close to the DVI connector as possible and the series termination resistors R2-R4 should be placed as close to the CH7301C as possible. If the analog outputs of the DVI-I connector are to be used, the ferrite beads L1-L8 should be placed as close to the DVI-I connector as possible to reduce EMI emissions.

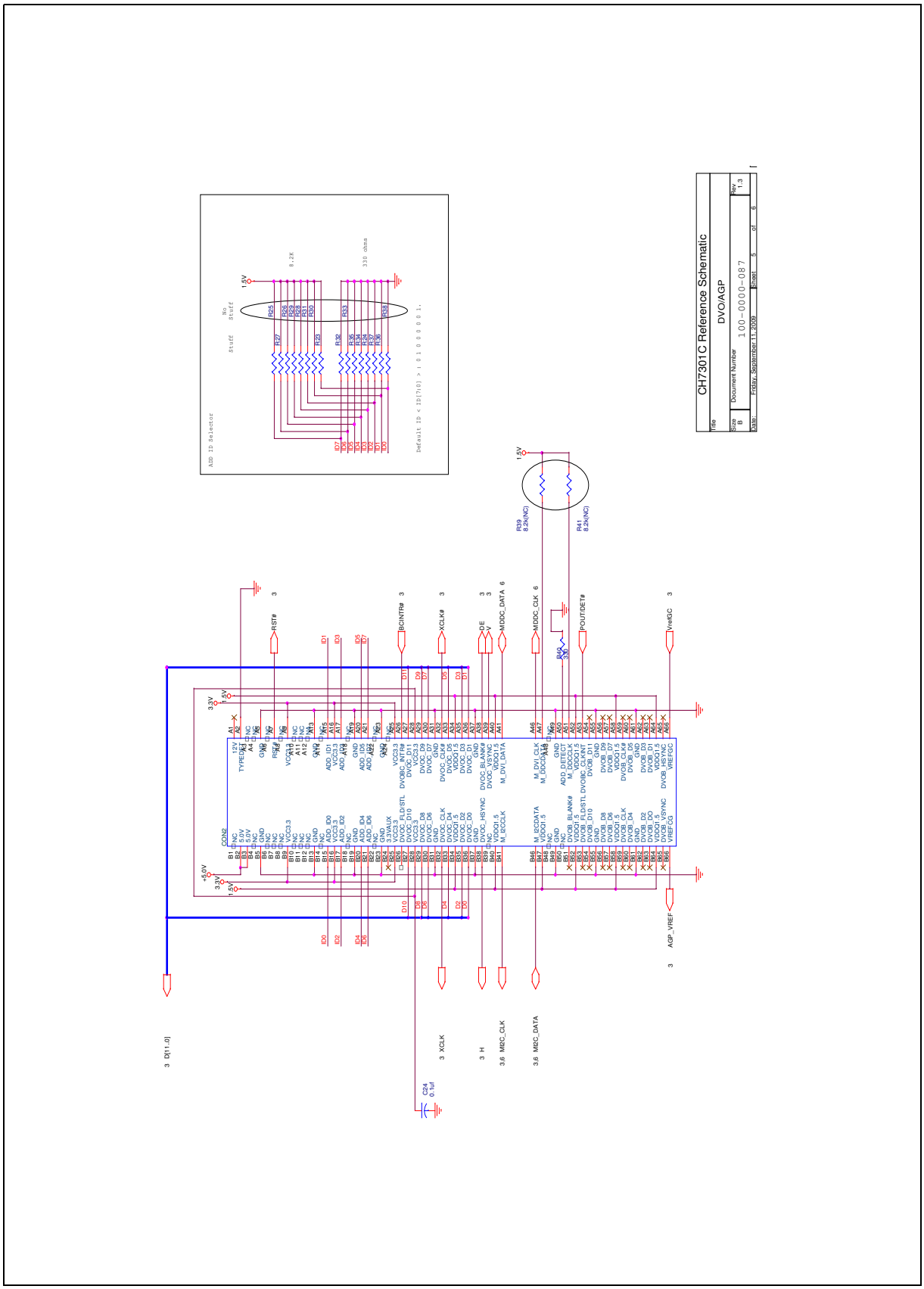
# 3. Reference Design Example

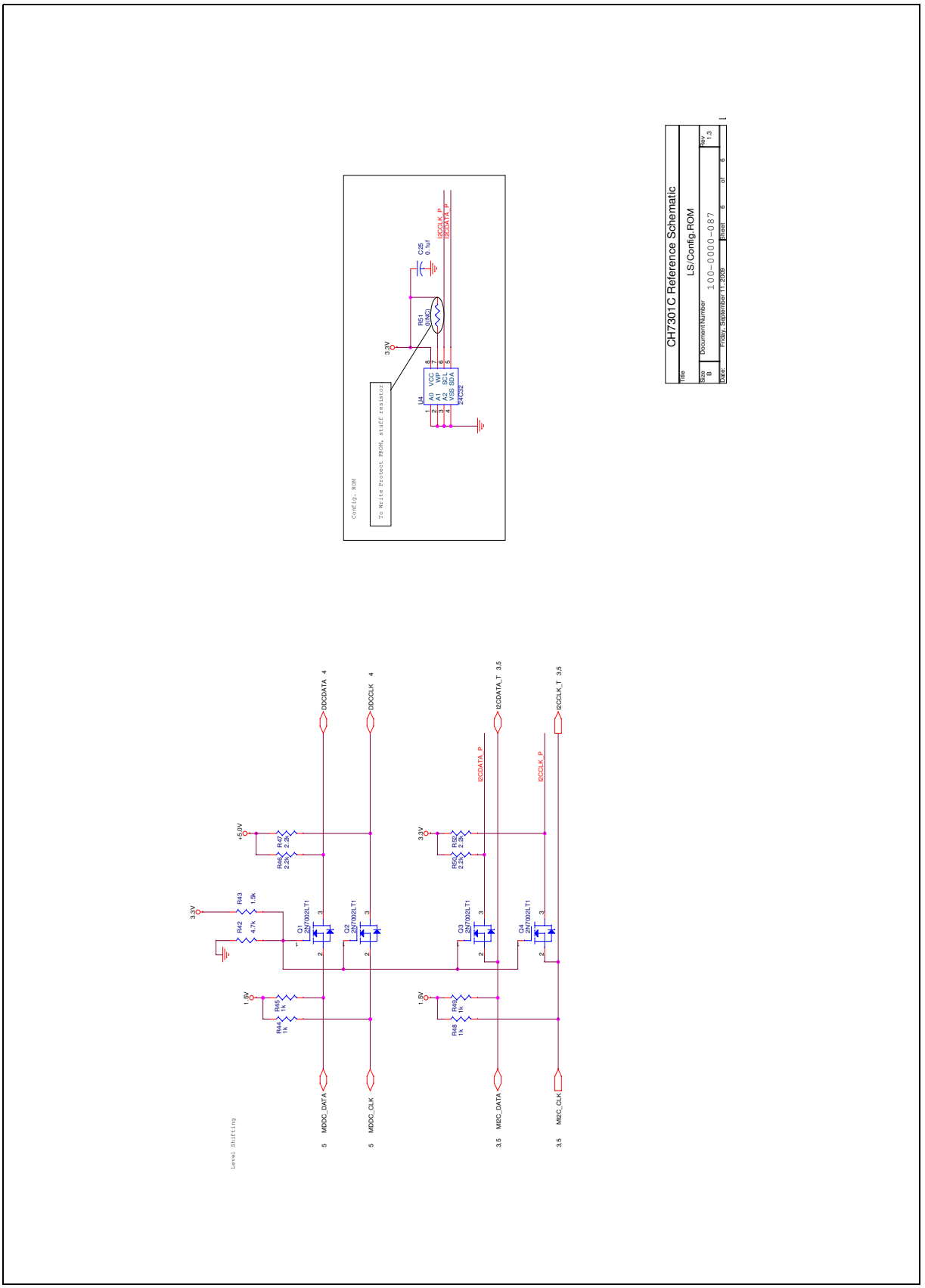
The following schematics are based on an Intel i845 / i855 / i865 Graphics chipset design and are to be used as a CH7301C PCB design example only. It is not a complete design. Those who are seriously doing an application design with CH7301C and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

## 3.1 Schematics of Reference Design Example


CH7301C Reference Schematic
CH7301C
100-0000-087
Keep these traces short and straight (top layer only with gnd on layer 2).
Route trace as 50 ohm line
I2C Address = 1110110
U1
CH7301C
HPDET
VSYNC
HSYNC
TEST
DVDD0
DVDD1
DVDD2
DGND0
DGND1
DGND2
DVDDV
TVDD0
TVDD1
TVDD2
TGND0
TGND1
TGND2
AVDD0
AGND1
VDD
GND0
GND1
VREF
ISET
VSWING
AS
GPIO1/HPINT
GPIO0
RESET*
SPD
SPC
XCLK*
XCLK
DE
H
V
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
TDO0*
TDO0
TDO1*
TDO1
TDO2*
TDO2
TLC*
TLC
L1 BEAD
L2 BEAD
L3 BEAD
L4 BEAD
C1 0.1uf
C2 0.1uf
C3 0.1uf
C4 47uf/10uf
C5 0.1uf
C6 0.1uf
C7 47uf/10uf
C8 0.1uf
C11 47uf/10uf
C12 0.1uf
C13 47uf/10uf
C14 0.1uf
C9 0.1uf(NC) Empty
C10 0.1uf(NC) Empty
R1 8.2k(NC)
R2 8.2k(NC)
R3 8.2k(NC)
R4 330
R5 330
R6 330
R7 140
R8 2.4K
R9
R10 10K(NC)
R11 10K(NC)
3.3V
1.5V
D[11:0]
XCLK#
XCLK
DE
H
V
RST#
I2CDATA_T
I2CCLK_T
AGP_VREF
BCINT#
VrefGC


CH7301C Reference Schematic
DVI Output
Document Number 100-0000-087
Monday, July 14, 2014
ESD Protection Diodes
Low capacitance, high speed ESD Protection Diodes for the DVI output is highly recommended. The Semtech 0514 is shown above.
EMI Stuffing Options:
A 68ohm and 0.5pF DVI output bridge circuit can be used further suppress electromagnetic emissions.
CON1
DVI-I
Semtech RClamp 0514
U2
U8
DDCCLK
DDCDATA
MONVSYNC
MONSCL
MONGREEN
MONBLUE
MONHSYNC
TDC2#
TDC2
TDC1#
TDC1
TLC#
TLC
TDC0
TDC0#


CH7301C Reference Schematic
DVO/AGP
100-0000-087
Friday, September 11, 2009
Default ID <ID[7:0]> : 01000001.
Add ID Selector
Stuff
No Stuff
8.2K
330 ohms
R39 8.2k(NC)
R41 8.2k(NC)
R40 0
1.5V
3.3V
5.0V
+5.0V
HRST#
BCINTR#
XCLK#
DE
MDDC_DATA
MDDC_CLK
POUTDET#
VrefGC
AGP_VREF
M2C_CLK
M2C_DATA
XCLK
H
D[11:0]
C24 0.1uf


CH7301C Reference Schematic
LS/Config.ROM
100-0000-087
Friday, September 11, 2009
Config. ROM
To Write Protect EROM, stuff resistor
U4
24C02
C25
0.1uf
R51
10K
3.3V
I2CCLK_P
I2CDATA_P
DDCDATA
DDCCLK
I2CDATA_T
I2CCLK_T
MDDC_DATA
MDDC_CLK
M2C_DATA
M2C_CLK
Level Shifting
+5.0V
1.8V
R40 2.2k
R41 2.2k
R42 4.7k
R43 1.5k
R44 1k
R45 1k
R46 1k
R47 1k
R48 1k
R49 1k
R50 2.2k
R52 2.2k
Q1 2N7002LT1
Q2 2N7002LT1
Q3 2N7002LT1
Q4 2N7002LT1

## 4. Revision History

| Revision | Date | Section | Description |
|---|---|---|---|
| 1.0 | 8/28/03 | All | First official release, Revision 1.0 |
| 1.1 | 9/14/09 | All | Updated ESD related information |
| 1.2 | 7/14/14 | Page5,9 | Modified the circuitry of HPDET. |

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